26th International Workshop on Post-Binary ULSI Systems (ULSIWS2017)

Tentative PROGRAM	
11:00-13:30	Registration & Lunch (12:00-:13:30)
13:30-13:40	Opening Remark *Local arrangement chair,* ***Jovanka Vanja Pantovic*** *(University of Novi Sad, Serbia)*
Invited Talk 1: Chair (TBD)	
13:40-14:20	Less is more- analog design with body gate biasing in 28nm UTBB FD-SOI ***Mirjana Videnovic-Misic*** *(Technical Sciences, Serbia)*
14:20-14:30	Brief Break
Invited Talk 2: Chair (TBD)	
14:30-15:10	MTJ-Based Nonvolatile FPGA; the Present and the Future Technology Trends ***Daisuke Suzuki*** *(Tohoku University, Japan)*
15:10-15:40	Coffee Break
Regular Session: Chair (TBD)	
15:40-16:00	Additional Parameters for Precise Estimation of ROBDD Complexity in Optimal Variable Order ***Milos Radmanovic*** *(University of Nis, Serbia)*
16:00-16:20	*TBD* ***Vincent Gaudet*** *(University of Waterloo, Canada)*
16:20-16:40	*On a Binarized / Ternarized Deep Neural Network Toward FPGA Realization* ***Hiroki Nakahara****, Haruyoshi Yonekawa (Tokyo Institute of Technology, Japan)*
16:40-16:50	Brief Break
Invited Talk 3: Chair (TBD)	
16:50-17:30	A digital circuit design for approximate computing ***Shimpei Sato*** *(Tokyo Institute of Technology, Japan)*
17:30-17:40	Closing *ULSIWS2017 General Co-chair,* ***Hiroki Nakahara*** *(Tokyo Institute of Technology, Japan)*
18:00-	ISMVL2017 Reception

40 minutes (including Q&A) for Invited Talk,
15 (Talk)+5(Q&A) minutes for Regular Session